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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,869	04/02/2001	Kevin J. McGrath	5500-64000	1001

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Lawrence J. Merkel
Conley, Rose, & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 02/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,869	MCGRATH ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2003 and 05 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 and 5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been examined.

Papers Received

2. Receipt is acknowledged of preliminary amendment, rescinding of non-publication notice, and both Information Disclosure Statements papers submitted, where the papers have been placed of record in the file.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> It states that priority to a provisional application is not applicable when there is in fact a claim for priority to provisional application 60/224,368.

Claim Objections

4. Claims 3 and 15 are objected to because of the following informalities: the claims use the phrase "...comprises one of a first size..." which is not permitted for a Markush group as shown in MPEP 2173.05(h). The examiner is taking the claim to mean, "...consists of one of a first size...".

> Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 6-12, 16, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 9 and 11 recite the limitation "said instruction's encoding" in lines 12 and 18 respectively. There is insufficient antecedent basis for this limitation in the claim. There is no previous introduction of an instruction's encoding in the claims. The examiner is taking the claims to mean, "an encoding of said instruction."

8. Claims 6, 12, 16, and 19 are objected to because of the following informalities: it is unclear what the "remainder" of the register is since it is not defined in the claims. The examiner is taking the "remainder" to simply be the standard definition of something leftover after other parts have been taken away so as to give it the broadest reasonable interpretation. Therefore, the remainder of the register is a leftover part of the register after other parts have been taken away.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Killian (5,420,992).

11. In regard to claim 1, Killian discloses a processor comprising:

a. A register (figure 1, element 42);

b. And an execution core (figure 1, execution unit) coupled to said register, wherein said execution core is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to selectively zero extend said result for update in said register responsive to an operand size corresponding to said instruction. Column 6, line 59 – column 7, line 7 show that the execution core (unit) executes instructions (performs operations) to produce a result that is written back to, or updates, the register. Column 12, lines 26-37 show that operands are zero extended to an operand size corresponding to an instruction. Figure 4A shows that the extender unit (120) performs on the result of the shifter unit (52) so the result is zero extended. Column 15, lines 61-64 show that the load unit produces this extended result as well.

12. In regard to claim 2, Killian discloses the processor as recited in claim 2, wherein said result comprises a number of bits specified by said operand size. As shown above, the operand size specifies a number of bits to zero-extend to.

13. In regard to claim 3, Killian discloses the processor as recited in claim 2, wherein said operand size consists of one of a first size, a second size greater than the first size, a third size greater than said second size, and a fourth size greater than said third size. Column 12, lines 28-37 give four operand sizes consisting of a first that is 8-bits (bytes), a larger second at 16-bits (halfwords), a still larger third at 32-bits (words), and a largest fourth at 64-bits (doublewords).

14. In regard to claim 4, Killian discloses the processor as recited in claim 3 wherein said register is capable of storing operands of said fourth size. As shown in column 12, lines 26-28, the registers are 64-bits wide and thus store operands of the fourth size.

15. In regard to claim 5, Killian discloses the processor as recited in claim 3 wherein said execution core is configured to zero extend said result if said operand size is said third size, and wherein said execution core is configured not to zero extend said result if said operand size is said first size or said second size. As shown above, the shift and load units zero extend the result of the third operand size. Tables 3A-4C show that the only instructions to zero extend are in fact certain shift and load instructions where the other instructions are not zero extended. Therefore, instructions of these types with the operand being of the first or second size will not have the result zero extended.

16. In regard to claim 6, Killian discloses the processor as recited in claim 5 wherein said execution core is configured to preserve a value in at least a portion of a remainder of said register if said operand size is said first size or said second size. It has been shown above that operands are of a first or second size. Since the remainder is a portion left over after other parts have been taken away, it follows that an instruction with the register as a source will take something away from the register. Since a read from a register does not change the contents of the register, this remainder is preserved.

17. In regard to claim 7, Killian discloses the processor as recited in claim 3 wherein said first size is eight bits, said second size is 16 bits, said third size is 32 bits, and said fourth size is 64 bits as shown above in the argument for claim 3

18. In regard to claim 8, Killian discloses the processor as recited in claim 1 wherein said execution core is coupled to receive an operating mode of said processor, and wherein said execution core is configures to selectively zero extend said result further responsive to said operating mode. Column 3, lines 38-55 show that an operating mode of the processor is received. It is also shown that these modes affect the sign and zero extending configurations as shown in column 3, line 56 – column 4, line 10. Thus the zero extend functionality is responsive to the operating modes.

19. In regard to claim 9, Killian discloses the processor as recited in claim 8, wherein said operating mode includes a default operand size, and wherein said operand size corresponding to said instruction is said default operand size unless overridden by an encoding of said instruction. The default operand size is specified as shown in column 3, lines 58-64, where the mode specifies the operand size via the instruction size of the program. As shown above, the operands are of four different sizes. In order to recognize the sizes, it is inherent that there is an encoding to specify the size.

20. In regard to claim 10, Killian discloses the processor as recited in claim 9 wherein said execution core is configured to zero extend said result if said operand size is said default operand size. Column 3, line 67 – column 4, line 10 shows that zero extending is performed in the given operating mode. The default operand size is specified as shown in column 3, lines 58-64, where the mode specifies the operand size via the instruction size of the program. Therefore the execution core is configured to zero extend if the operand size is the default.

21. In regard to claim 11, Killian discloses the processor as recited in claim 9 wherein said default operand size is overridden by an encoding in said instruction if said instruction includes one or more operand size prefixes. As shown above, the operands are of four different sizes. In order to recognize the sizes, it is inherent that there is an encoding to specify the size. A prefix is interpreted as being a set of bits. Since the instruction is a set of bits with an encoding then there is an operand size prefix included in the instruction.

22. In regard to claim 12, Killian discloses the processor as recited in claim 1 wherein said execution core is configured to preserve a value in at least a portion of a remainder of said register if not zero extending said result. Since the remainder is a portion left over after other parts have been taken away, it follows that an instruction with the register as a source will take something away from the register. Since a read from a register does not change the contents of the register, this remainder is preserved regardless of if the result is zero extension, and thus preserved if the result is not zero extended.

23. In regard to claim 13, Killian discloses a method comprising:

a. Executing an instruction to produce a result, said instruction having a register as a destination; Column 6, line 59 – column 7, line 7 show that the execution core (unit) executes instructions (performs operations) to produce a result that is written back to, or updates, a register.

b. And selectively zero extending said result for update in said register responsive to an operand size corresponding to said instruction. Column 12,

lines 26-37 show that operands are zero extended to an operand size corresponding to an instruction. Figure 4A shows that the extender unit (120) performs on the result of the shifter unit (52) so the result is zero extended. Column 15, lines 61-64 show that the load unit produces this extended result as well.

24. In regard to claim 14, Killian discloses the method as recited in claim 13, wherein said result comprises a number of bits specified by said operand size. As shown above, the operand size specifies a number of bits to zero-extend to.

25. In regard to claim 15, Killian discloses the method as recited in claim 14,

a. wherein said operand size consists of one of a first size, a second size greater than the first size, a third size greater than said second size, and a fourth size greater than said third size. Column 12, lines 28-37 give four operand sizes consisting of a first that is 8-bits (bytes), a larger second at 16-bits (halfwords), a still larger third at 32-bits (words), and a largest fourth at 64-bits (doublewords).

b. and wherein said selectively zero extending comprises:

i. zero extend said result if said operand size is said third size;

ii. and not zero extending said result if said operand size is said first size or said second size

As shown above, the shift and load units zero extend the result of the third operand size. Tables 3A-4C show that the only instructions to zero extend are in fact certain shift and load instructions where the other instructions are not zero

extended. Therefore, instructions of these types with the operand being of the first or second size will not have the result zero extended.

26. In regard to claim 16, Killian discloses the method as recited in claim 15 further comprising preserving a value in at least a portion of a remainder of said register if said operand size is said first size or said second size. It has been shown above that operands are of a first or second size. Since the remainder is a portion left over after other parts have been taken away, it follows that an instruction with the register as a source will take something away from the register. Since a read from a register does not change the contents of the register, this remainder is preserved.

27. In regard to claim 17, Killian discloses the method as recited in claim 13 wherein said selectively zero extending is further responsive to an operating mode of a processor performing said execution. Column 3, lines 38-55 show operating modes of a processor. It is also shown that these modes affect the sign and zero extending configurations as shown in column 3, line 56 – column 4, line 10. Thus the zero extend functionality is responsive to the operating modes.

28. In regard to claim 18, Killian discloses the method as recited in claim 17 wherein said operating mode includes a default operand size, and wherein zero extending further comprises zero extending said result if said operand size is said default operand size. The default operand size is specified as shown in column 3, lines 58-64, where the mode specifies the operand size via the instruction size of the program. Column 3, line 67 – column 4, line 10 shows that zero extending is performed in the given operating mode. The default operand size is specified as shown in column 3, lines 58-

64, where the mode specifies the operand size via the instruction size of the program. Therefore the execution core is configured to zero extend if the operand size is the default.

29. In regard to claim 19, Killian discloses the method as recited in claim 13 further comprising preserving a value in at least a portion of a remainder of said register if not zero extending said result. Since the remainder is a portion left over after other parts have been taken away, it follows that an instruction with the register as a source will take something away from the register. Since a read from a register does not change the contents of the register, this remainder is preserved regardless of if the result is zero extension, and thus preserved if the result is not zero extended.

Conclusion

30. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references have been cited to further show the art with respect to zero extending in general.

US Pat No 5,907,694 to Suzuki discloses a processor and method for operating that zero extends results based on four different operand sizes.

US Pat No 5,091,853 to Watanabe teaches zero extension based on three different operand sizes as well as processing modes.

US Pat No 5,227,989 to Jones shows an execution core that uses zero extension for different instructions' execution.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
February 3, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100